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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,365	08/31/2001	Jun Osanai	S004-4393	1289

7590 11/04/2003

ADAMS & WILKS
31st Floor
50 Broadway
New York, NY 10004

EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,365	OSANAI ET AL.	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-93* is/are pending in the application.

4a) Of the above claim(s) *3,5-10,12-14,17-42,44-53,55-73 and 77-82* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,11,15,16,43,54,74-76,83 and 87-90* is/are rejected.

7)☒ Claim(s) *84-86 and 91-93* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Claims 77-82 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 8.

Claim Objections

Claim 1 is objected to because of the following informalities: line 8 "in" should --on--. Appropriate correction is required.

Claim 4 is objected to because of the following informalities: line 2 "of" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 43 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of "regions of the N-channel MOS transistor and the P-channel MOS transistor are formed in an N-type well" sets forth

structure not supported by the disclosure. In fact, Fig 1 of elected embodiment shows region 113 of the N-channel MOS transistor is not formed in an N-type well.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 11, 15, 16, 43, 54, 74-76, 83 and 87-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erdeljac et al. (USPN 5,554,873) in view of Yoh et al. (USPN 4,559,694).

Erdeljac et al. discloses a complementary MOS semiconductor device (Fig. 11) comprising a semiconductor substrate; a CMOS transistor pair comprised of an N-channel MOS transistor 44 in the semiconductor substrate and a P-channel MOS transistor 50 formed in the semiconductor substrate, both the transistor 44 and the transistor 50 forming a complementary transistor pair; and a resistor formed on the semiconductor substrate. Erdeljac et al. does not disclose a conductivity type of a gate electrode 24 of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode 24 of the P-channel MOS transistor is P-type. Yoh et al. discloses a complementary MOS semiconductor device (Figs. 59, 60) having an N-channel MOS transistor Q4, a P-channel MOS transistor Q1, wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type. It would have been obvious to a

person having ordinary skill in the art at the time the invention was made to form the gate electrodes 24 of the P-channel MOS transistor 50 and the N-channel MOS transistor 44 doped of P-type as taught by Yoh et al. instead of N-type in order to obtain transistors having low threshold voltages that operate at low voltage and consume low power.

Regarding claims 2, 74-76, the gate electrodes 24 each comprises a single layer of polysilicon having a film thickness of about 5000 angstroms. Yoh et al. discloses boron served as a P-type impurity and P-type gate electrode having an impurity concentration of $1x10^{19}$ atoms/cm^3 or more. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope boron in the P-type gate electrodes 24 of MOS transistors 44 and 50 with an impurity concentration of $1x10^{19}$ atoms/cm^3 or more as taught by Yoh et al. in order to increase the gate electrode conductivity and to obtain transistors having low threshold voltages that operate at low voltage and consume low power.

Regarding claim 4, the resistor 32 is a polysilicon resistor having the same film thickness as a polysilicon constituting the gate electrodes 24.

Regarding claim 11, the N-channel MOS transistor 44 and the P-channel MOS transistor 50 have a single drain structure comprising a diffusion layer with a high impurity concentration, and a source (42, 48) and a drain (42, 48) overlap the P-type gate electrode 24 in a planar manner.

Regarding claim 15, the N-channel MOS transistor 44 has p-type gate electrode which is the same transistor as claimed; therefore, the N-channel MOS transistor 44 inherently has a buried channel and a threshold voltage in an enhancement mode.

Regarding claim 16, 83 and 90, the P-channel MOS transistor 50 has p-type gate electrode which is the same transistor as claimed; therefore, the P-channel MOS transistor 44 inherently has a surface channel and a threshold voltage in an enhancement mode.

Regarding claim 43, the modify Erdeljac et al. discloses a P-type semiconductor substrate 10, and a region of the P-channel MOS transistor 50 is formed in an N-type well 18 in the semiconductor substrate.

The claim limitations "formed in the same layer" in claim 4 and "formed by chemical vapor deposition" in claim 54 are taken to be product by process limitations. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a " product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claims 87-88, the claim limitations "is used in a reference voltage generating circuit of a voltage regulator", "is used as an output driving transistor of the voltage regulator" in claim 87; "for a voltage regulator", "used in a reference voltage generating circuit of the voltage regulator" and "used as an output element of the voltage regulator" in claim 88; "for a voltage regulator", "serving as the output driving transistor of the voltage regulator", "used in the voltage divider" in claim 89 specify an intended use or field of use. It has been held that in device claims, intended use must result in a structural difference between the claim invention and the prior art in order to patentably distinguish the claim invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

Furthermore, Erdeljac et al. in view of Yoh et al. does not explicitly disclose the N-channel MOS transistor 44 being used in a reference voltage generating circuit of a voltage regulator, the P-channel MOS transistor 50 being used as an output driving of the voltage regulator and the resistor being used in the voltage divider. A voltage regulator having a reference voltage generating circuit, an error amplifier, an output driving transistor and a voltage divider is a conventional device. It would have been obvious to form the structure of Erdeljac et al. in view of Yoh et al. as part of the

conventional voltage regulator wherein the N-channel MOS transistor 44 being used in a reference voltage generating circuit of the conventional voltage regulator, the P-channel MOS transistor 50 being used as an output driving of the voltage regulator and the resistor being used in the voltage divider for the advantages that the modified structure of Erdeljac et al. provides as described above.

Allowable Subject Matter

Claims 84-86 and 91-93 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 08/04/2003 have been fully considered but they are not persuasive.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

In response to applicant's argument that Yoh fails to disclose transistors formed together as complementary MOS transistors, applicant's argument is not a fact and cannot replace evidence where evidence is necessary. It is clear that both prior art references disclose CMOS transistor pair comprising an N-channel MOS transistor and a P-channel MOS transistor.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
October 31, 2003

Thien F Tran

Thien F Tran
Primary Examiner
Art Unit 2811